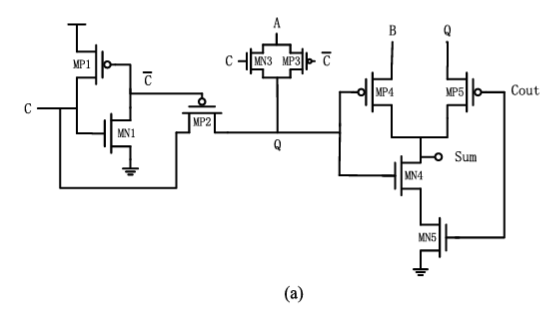
**PROJECT BASED LEARNING**

**CEC370 – LOW POWER IC DESIGN**

**Project 1 :**

1. (i) Design the approximate 1 bit full adder (LCAFA-1) given below using Cadence Virtuoso for 45nm technology



(ii) Determine the Error metrics – ED, ER(Sum), ER(Cout), RED

(ii) Simulate the adder and determine the Average Power dissipated and Propagation delay of the 1 bit full adder

(iii) Convert the 1-bit full adder into a symbol and realize 8-bit Carry save adder(CSA). Simulate the CSA.

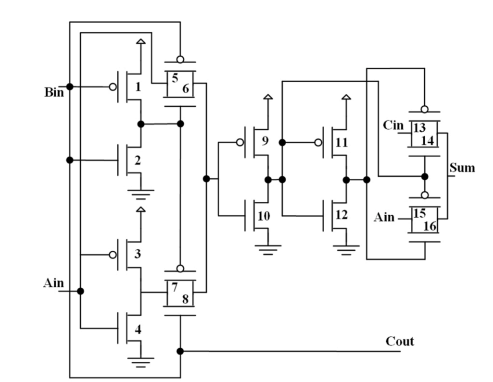
(iv) Application : Read 2 images from matlab . It should be converted to .scs file and fed as inputs to adder in Virtuoso. Simulate in Cadence and pool the results back to MATLAB and read the output images. Determine PSNR, SSIM

**Team Members :**

* **Mythili.S**
* **JAWAHAR V**
* **Joel Davis**
* **SANTO FLYNN S**

**Project 2 :**

1. (i) Design the approximate 1 bit full adder (TGA-I) given below using Cadence Virtuoso for 45nm technology



(ii) Determine the Error metrics – ED, ER(Sum), ER(Cout), RED

(ii) Simulate the adder and determine the Average Power dissipated and Propagation delay of the 1 bit full adder

(iii) Convert the 1-bit full adder into a symbol and realize 8-bit Carry save adder(CSA). Simulate the CSA.

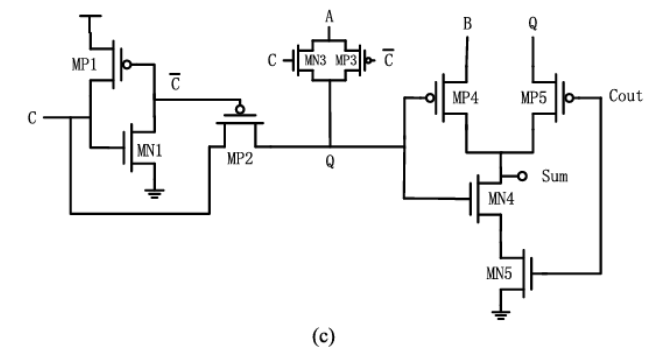
(iv) Application : Read 2 images from matlab . It should be converted to .scs file and fed as inputs to adder in Virtuoso. Simulate in Cadence and pool the results back to MATLAB and read the output images. Determine PSNR, SSIM

**Team Members :**

* **Karthikeyan**
* **Bharathan**
* **DHINAKARAN A**
* **R.SESHANTH**

**Project 3 :**

1. (i) Design the approximate 1 bit full adder (LCAFA-3) given below using Cadence Virtuoso for 45nm technology



(ii) Determine the Error metrics – ED, ER(Sum), ER(Cout), RED

(ii) Simulate the adder and determine the Average Power dissipated and Propagation delay of the 1 bit full adder

(iii) Convert the 1-bit full adder into a symbol and realize 8-bit Carry save adder(CSA). Simulate the CSA.

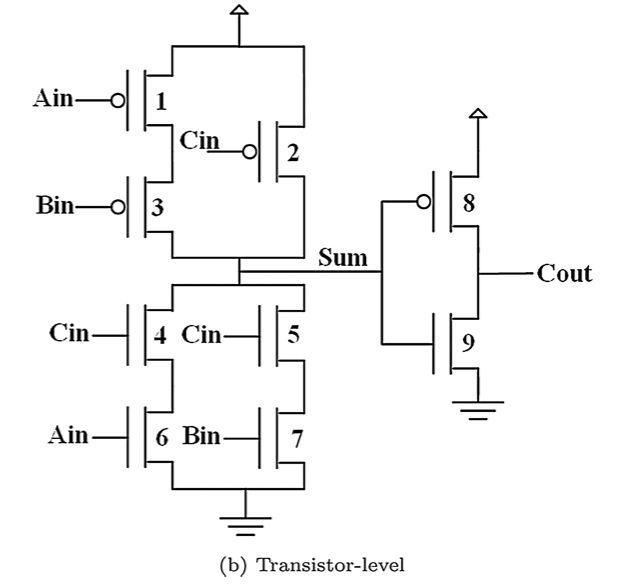
(iv) Application : Read 2 images from matlab . It should be converted to .scs file and fed as inputs to adder in Virtuoso. Simulate in Cadence and pool the results back to MATLAB and read the output images. Determine PSNR, SSIM

**Team Members :**

* **Mohammed Meeran Almatheen N**
* **Moses Marvin J**
* **Merlin Zeetha A**

**Project 4 :**

1. (i) Design the approximate 1 bit full adder (LAHAF) given below using Cadence Virtuoso for 45nm technology



(ii) Determine the Error metrics – ED, ER(Sum), ER(Cout), RED

(ii) Simulate the adder and determine the Average Power dissipated and Propagation delay of the 1 bit full adder

(iii) Convert the 1-bit full adder into a symbol and realize 8-bit Carry save adder(CSA). Simulate the CSA.

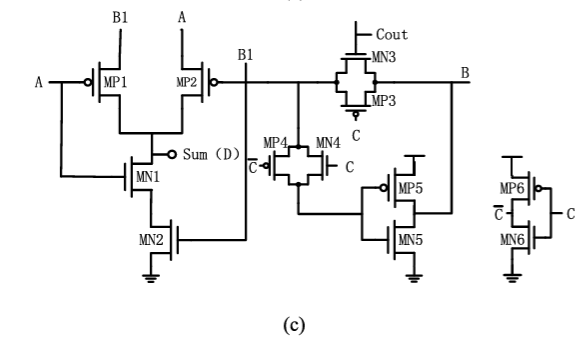
(iv) Application : Read 2 images from matlab . It should be converted to .scs file and fed as inputs to adder in Virtuoso. Simulate in Cadence and pool the results back to MATLAB and read the output images. Determine PSNR, SSIM

**Team Members :**

* **Arul Austina**
* **Sandeep A Raymond**
* **AGNES CHRISTINA FERNANDEZ**

**Project 5 :**

1. (i) Design the approximate 1 bit full adder (LCAFA7) given below using Cadence Virtuoso for 45nm technology



(ii) Determine the Error metrics – ED, ER(Sum), ER(Cout), RED

(iii) Simulate the adder and determine the Average Power dissipated and Propagation delay of the 1 bit full adder

(iv) Convert the 1-bit full adder into a symbol and realize 8-bit Carry save adder(CSA). Simulate the CSA.

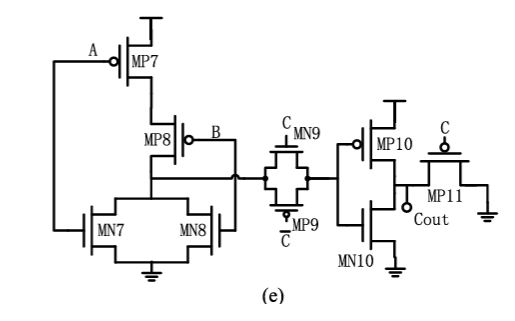
(v) Application : Read 2 images from matlab . It should be converted to .scs file and fed as inputs to adder in Virtuoso. Simulate in Cadence and pool the results back to MATLAB and read the output images. Determine PSNR, SSIM

**Team Members :**

* **S.MUHAMMAD JAMALDEEN**
* **Manoj**
* **SRI YOGESHWARAN.S**

**Project 6 :**

1. (i) Design the approximate 1-bit full adder (LCAFA8) given below using Cadence Virtuoso for 45nm technology



(ii) Determine the Error metrics – ED, ER(Sum), ER(Cout), RED

(ii) Simulate the adder and determine the Average Power dissipated and Propagation delay of the 1 bit full adder

(iii) Convert the 1-bit full adder into a symbol and realize 8-bit Carry save adder(CSA). Simulate the CSA.

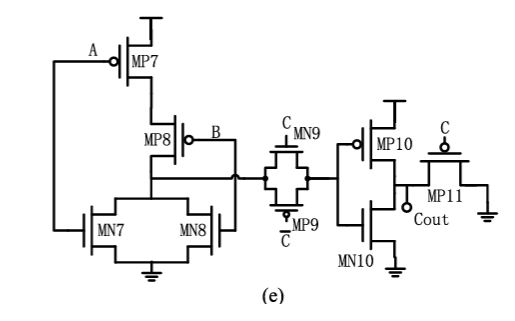
(iv) Application : Read 2 images from matlab . It should be converted to .scs file and fed as inputs to adder in Virtuoso. Simulate in Cadence and pool the results back to MATLAB and read the output images. Determine PSNR, SSIM

**Team Members :**

* **S.Bernish Daniel**
* **S Phinehas Samuel**
* **A ANTONY RICHARD**

**Project 7 :**

1. (i) Design the approximate 1-bit full adder (LCAFA8) given below using Cadence Virtuoso for 45nm technology



(ii) Determine the Error metrics – ED, ER(Sum), ER(Cout), RED

(ii) Simulate the adder and determine the Average Power dissipated and Propagation delay of the 1 bit full adder

(iii) Convert the 1-bit full adder into a symbol and realize 8-bit Carry save adder(CSA). Simulate the CSA.

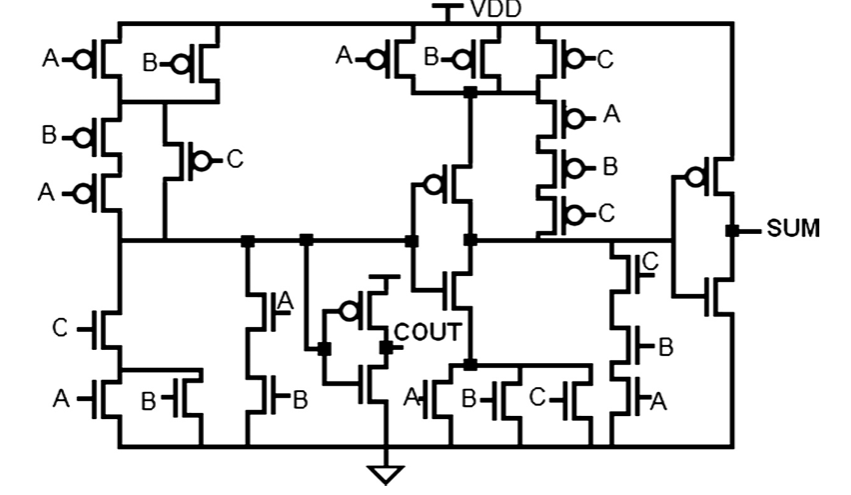
(iv) Application : Read 2 images from matlab . It should be converted to .scs file and fed as inputs to adder in Virtuoso. Simulate in Cadence and pool the results back to MATLAB and read the output images. Determine PSNR, SSIM

**Team Members :**

* **Architha R**
* **Aparna S M**
* **Joseph Deepan J**
* **SHIRIN MARIA PRIYA.W**

**Project 8 :**

1. (i) Design the Accurate 1-bit full adder given below using Cadence Virtuoso for 45nm technology



(ii) Simulate the adder and determine the Average Power dissipated and Propagation delay of the 1 bit full adder

(iii) Convert the 1-bit full adder into a symbol and realize 8-bit Carry save adder(CSA). Simulate the CSA.

(iv) Application : Read 2 images from matlab . It should be converted to .scs file and fed as inputs to adder in Virtuoso. Simulate in Cadence and pool the results back to MATLAB and read the output images. Determine PSNR, SSIM

**Team Members :**

* **MARIA REENA J**
* **R.JASMINE THABITHA**
* **G. SRI YASHWANTHAN**
* **Maria Jenita L**